## Application Note AN002

# Precautions required to use SPI/QPI Flash Memory with GAP8

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#### **SUMMARY**

GAP8-centric application boards that use SPI/QPI Flash may need to implement a weak pull-up resistor on pin SDIO3/RESET#/HOLD#. This is typically the case for SPI Flashes housed in 8-pin package.

### **INTRODUCTION**

GAP8 offers the option to boot from a Flash connected to its SPI bus (SPIM0 interface).

This interface supports single as well as quad-SPI a.k.a QPI, whereby the data can be transfered over 4 lines (SDIO0-3) rather than a single line. GAP8 can therefore boot from and exchange data with QPI-capable Flashes, thus enabling to reach greater data transfer rate than with single QPI.

However, when using a QPI Flash, some precautions may be required to ensure proper operation at sytem level. Here is an explaination.

### **RATIONALE**

- > When GAP8 boots from external SPI Flash, it starts up with a « conservative » approach, in single SPI mode with basic read opcodes, in order to allow usage of a large selection of Flash models. (The secondary boot code obtained from those initial Flash access would then normally switch to a faster operation mode). In single SPI mode, GAP8 does not drive SDIO2 and SDIO3 pins.
- > On the other hand, some Quad-SPI capable Flashes multiplex a HOLD#/RESET# signal with the SDIO3 signal on the same pin ("SDIO3/HOLD#/RESET#"). This is commonly the case with low pin count Flashes housed in an 8-pin package.

In single SPI mode, SDIO3 functionality is not relevant and either HOLD# (default) or RESET# (configurable alternative) functionality is enabled: asserting HOLD# or RESET# diverts the Flash from its normal operation (see Flash datasheet for details).

> Therefore, if you just connect such a Flash to GAP8 then at initial power-up the SDIO3/HOLD#/RESET# pin is floating and can randomly switch to 0 or 1. If it's seen as Logic1 by the Flash, the Flash is not disturbed and things proceed normally. However if it is seen as Logic0, then the Flash gets disturbed and Flash accesses fail.

### **CONCLUSION**

To avoid this situation, if your board uses a Flash that multiplex HOLD#/RESET# with SDIO3 (usually the case for 8-pin Flashes), then it is required to provision a weak pull-up (for example 50-100 Kohm) on SDIO3 (Fig. 1).

FLASH MEMORY

CE# VCC 50-100 Kohm

SDIO1 SDIO3/RST#/HOLD#

SDIO2 / WP# SCK

GND SDIO0

Fig.1: 8-pin Flash with shared SDIO3#